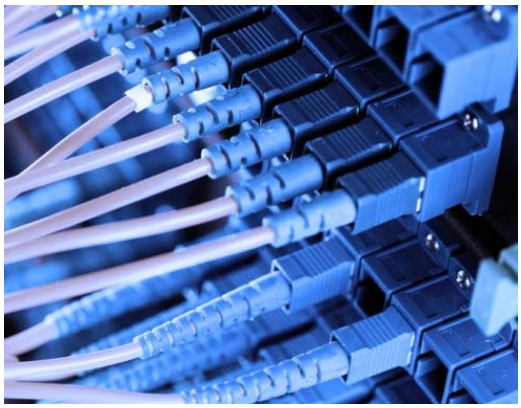
Product Brief
RS1010
10G Ethernet MAC



The Rianta Solutions RS1010 10G Ethernet MAC block is fully verified IP suitable for integration into FPGA or ASIC solutions for multiple packet applications. Implemented in Verilog with comprehensive testbench support, the RS1010 includes a full MAC, Reconciliation Sublayer (RS) and XGMII Extender Sublayer (XGXS) complete with RMON/MIB statistics and Ethernet OAM support.

Interfaces

- System Data
  - Flexible Rx and Tx Data Packet FIFOs
- RS
  - XGMII
- XGXS
  - XAUI
- Management
  - Serial or parallel Address/Data
  - Access to EOAM Tx/Rx FIFOs

Applications

- Packet Processing
  - Switching
  - Routing
- Packet Transport
  - Packet Optical Transport Systems (POTS)

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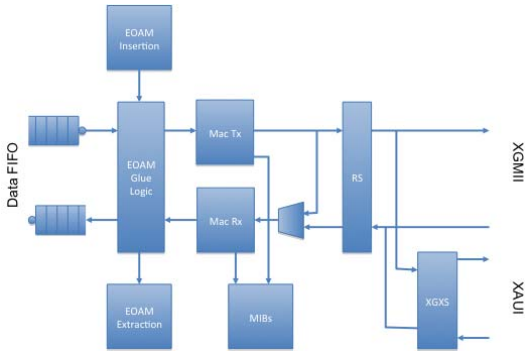
Features

- RS
  - XGMII interface to local PCS
    - 32-bit Data
    - 4-bit Control
  - Detection/generation of fault codes and control characters
  - Alignment of start control character to XGMII lane 0
  - Deficit Idle Counter implementation
  - Full duplex
- XGXS
  - XAUI interface to remote PCS
  - 8B/10B encoding/decoding of XGMII lanes
  - interframe insertion/deletion for clock compensation
- MAC
  - Wire speed CRC-32 verification in Rx direction
    - Optional frame discard on failure
  - Optional CRC-32 insertion in Tx direction
  - PAUSE Frame based flow control
    - Automatic generation based on configurable Rx FIFO thresholds
    - S/W controlled generation
    - Configurable PAUSE quanta
  - 64-16000 byte frame size
  - Full RMON MIB statistics
  - Ethernet OAM frame insertion and capture
    - Flexible capture match field with bit mask
      - Covers DA, Type/Info, Q tag

Block Diagram



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Description

The Rianta Solutions RS1010 10G Ethernet MAC is a flexible IP core which can be integrated into a variety of applications requiring Ethernet connectivity. Providing a dedicated MAC/RS implementation, the RS1010 can interface either directly or remotely to a PMA/SerDes on the line side, and to any transport or switching function on the system side.

The RS/XGXS interface operates as either XGMII (clocked 32-bit data + 4 bit control) or XAUI (clockless 4 lane serial) to interface to a variety of 10G PMA/PMD implementations. On the system side, simple transmit and receive FIFOs are provided with configurable thresholds for automatic flow control along with access to absolute pointer locations to manage fill levels. Parallel and serial control interfaces are also provided for access to all control and status registers as well as EOAM insertion/extraction buffers.

Implemented in Verilog RTL, the RS1010 is fully verified with a high level test suite that can also be integrated into system test scenarios.

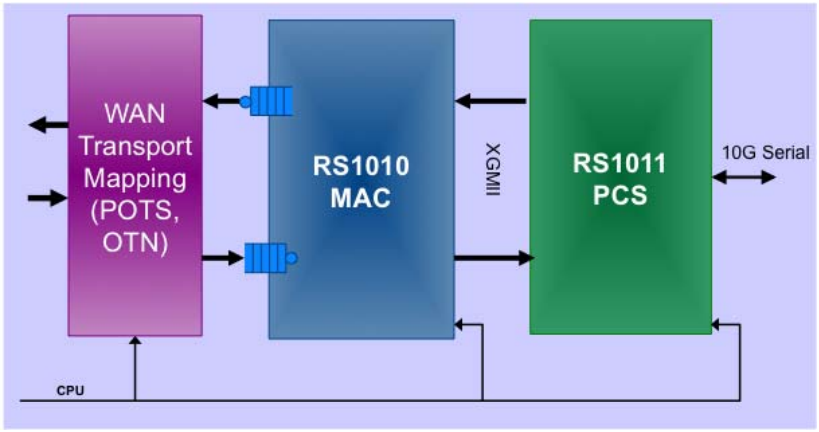

Figure 1: 10G Ethernet MAC/PCS Direct Connection

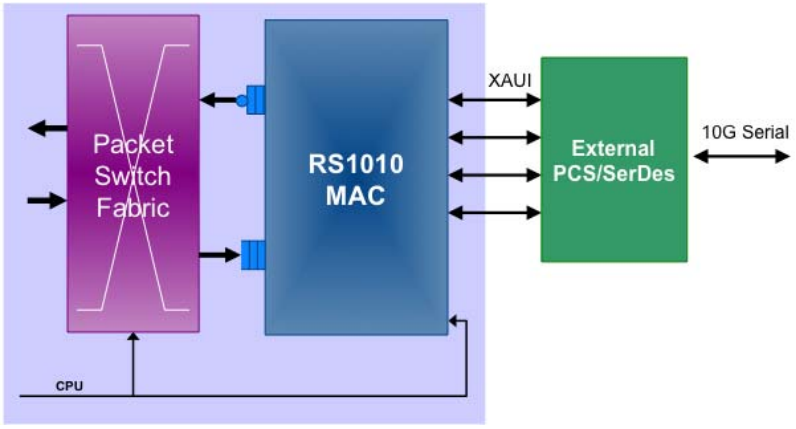

Figure 2: 10G Ethernet MAC/PCS Remote Connection