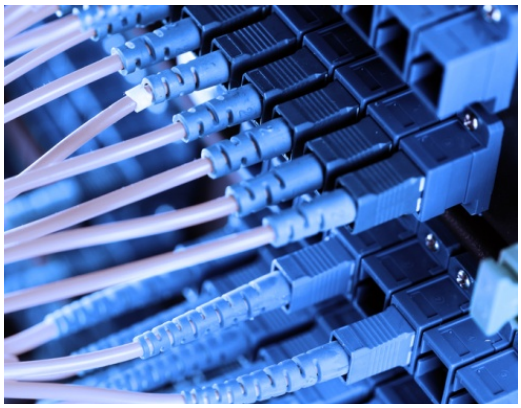
Product Brief
RS1011
10GBASE-W/R/X/T PCS



The Rianta Solutions RS1011 10GBASE-W/R/X/T PCS block is fully verified IP suitable for integration into FPGA or ASIC solutions for multiple packet applications. Implemented in Verilog with comprehensive testbench support, the RS1011 includes a configurable PCS supporting all 10GBASE types. In addition, the RS1011 supports both direct and remote connection to a Reconciliation Sublayer (RS) via XGMII or XAUI.

Interfaces

- RS
  - XGMII or XAUI
- PMA/PMD
  - Encoded 10B, 65B or 66B
- Management
  - Serial or parallel Address/Data

Applications

- Packet Processing
  - Switching
  - Routing
- Packet Transport
  - Packet Optical Transport Systems (POTS)

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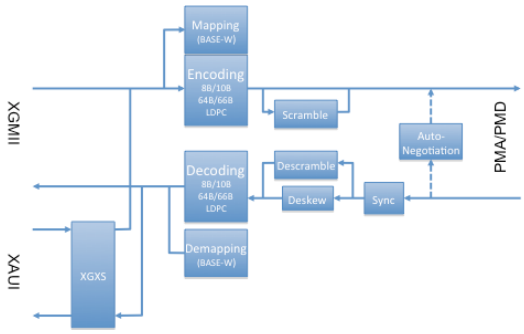
Features

- Optional XGXS
  - XAUI Interface to remote RS
  - 8B/10B encoding/decoding of XGMII lanes
  - interframe insertion/deletion for clock compensation
- XGMII interface to local RS
  - 32-bit Data
  - 4-bit Control
- 10GBASE-W/R
  - 64B/66B encoding/decoding (10GBASE-W/R)
  - Scrambling/descrambling (10GBASE-R)
  - WIS encapsulation (10GBASE-W)
- 10GBASE-X
  - 8B10B encoding/decoding
- 10GBASE-T
  - LDPC encoding/decoding
  - Scrambling/descrambling
  - Auto-negotiation
- Detection and generation of fault and control codes
- Full duplex
- Loopback and test pattern support

Block Diagram



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Description

The Rianta Solutions RS1011 10GBASE-W/R/X/T PCS is a flexible IP core which can be integrated into a variety of applications requiring Ethernet connectivity. Providing a complete PCS implementation, the RS1011 can interface directly to a PMA/SerDes implementation on the line side and to a local or remote MAC/RS function on the system side.

The line interface operates with 10B (8B10B encoded), 65B (LDPC encoded) or 66B (64B/66B encoded) blocks to interface to a variety of 10G PMA/PMD implementations. On the system side, either a clocked XGMII or clockless XAUI interface can be used. Parallel and serial control interfaces are also provided for access to all control and status registers as well as EOAM insertion/extraction buffers.

Implemented in Verilog RTL, the RS1011 is fully verified with a high level test suite that can also be integrated into system test scenarios.

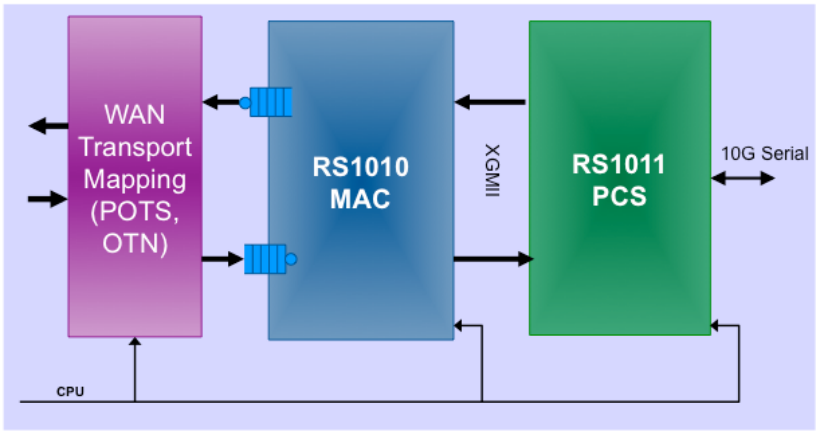

Figure 1: 10G PCS/MAC Implementation

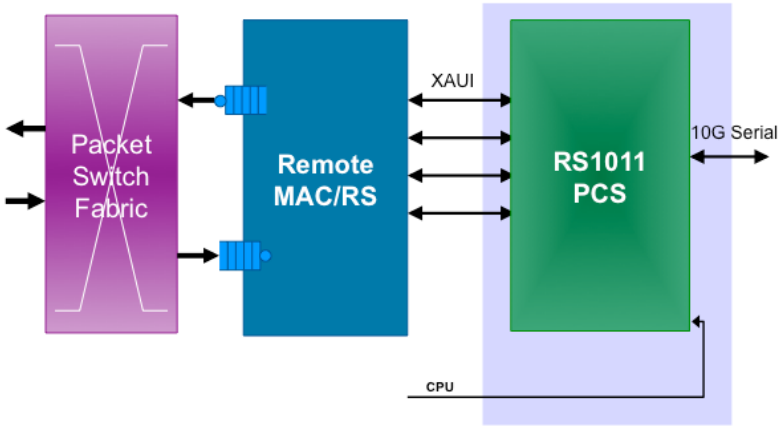

Figure 2: 10G PCS with remote MAC