

The Rianta Solutions RS1110 10/100/1000 Ethernet MAC/PCS/PMA block is fully verified IP suitable for integration into Packet Processing or Packet Transport FPGA or ASIC solutions. Implemented in Verilog with comprehensive testbench support, the RS1110 includes a complete tri-rate MAC and PCS/PMA implementation complete with RMON/MIB statistics and Ethernet OAM.

### Interfaces

- System Data
  - Flexible Rx and Tx Data FIFOs
- SerDes
  - 4/5/8/10/16/20 bit interface
- Management
  - Serial or parallel Address/Data
  - Access to EOAM Tx/Rx FIFOs

### Applications

- Packet Processing
  - Switching
  - Routing
- Packet Transport
  - Ethernet over SONET/SDH/PDH
  - Packet Optical Transport Systems (POTS)

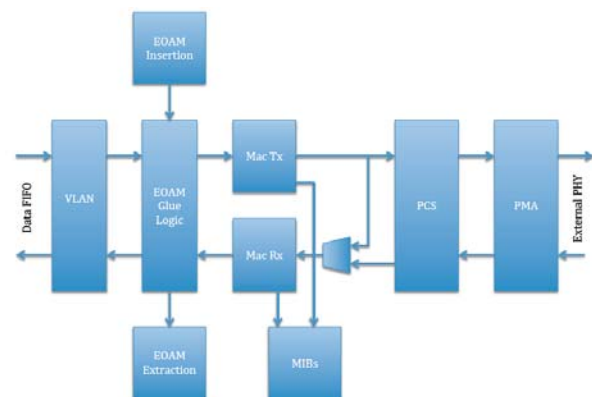
## RS1110

### 10/100/1000 Ethernet MAC/PCS/PMA

#### Features

- Tri-rate PCS/PMA
  - Configurable 8B10B (GE), 4B5B (FE) and Manchester (E) line codes
  - Detection and generation of fault codes
  - Full duplex
- Tri-rate MAC
  - Wire speed CRC-32 verification in Rx direction
    - Optional frame discard on failure
  - Optional CRC-32 insertion in Tx direction
  - PAUSE Frame based flow control
    - Automatic generation based on configurable Rx FIFO thresholds
    - S/W controlled generation
    - Configurable PAUSE quanta
    - Optional forwarding of received PAUSE Frames to application or automatic response with Tx PAUSE indication to application
- 802.1Q VLAN processing
  - Class of Service and Scheduling
- 64-16000 byte frame size
- Full RMON MIB statistics
- Ethernet OAM frame insertion and capture
  - Flexible capture match field with bit mask
    - Covers DA, Type/Info, Q tag

### Block Diagram

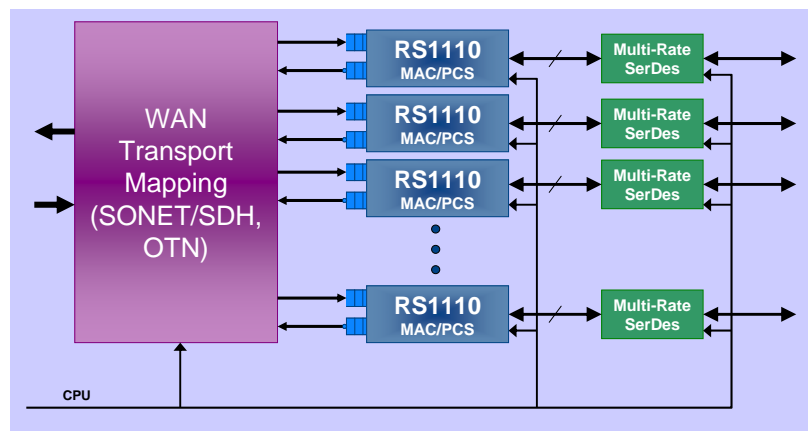


**Description**

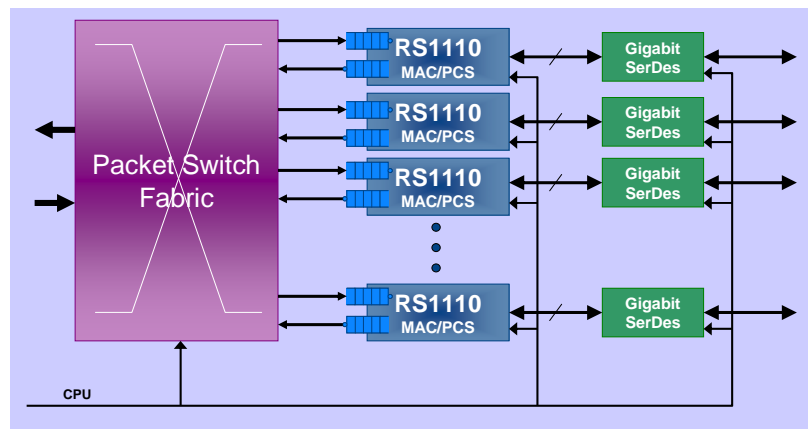
The Rianta Solutions RS1110 10/100/1000 Ethernet MAC/PCS is a flexible IP core which can be integrated into a variety of applications requiring Ethernet connectivity. Providing a combined MAC and PCS implementation, the RS1110 can interface to single or multi-rate SerDes on the line side, and to any transport or switching function on the system side.

The SerDes interface can be configured for a variety of bit widths to simplify multi-rate designs. On the system side, simple transmit and receive FIFOs are provided with configurable thresholds for automatic flow control along with access to absolute pointer locations to manage fill levels. Parallel and serial control interfaces are also provided for access to all control and status registers as well as EOAM insertion/extraction buffers.

Implemented in Verilog RTL, the RS1110 is fully verified with a high level test suite that can also be integrated into system test scenarios.



**Figure 1: Multi-Port, Multi-Rate Ethernet Transport**



**Figure 2: Multi-Port Gigabit Ethernet Switching**

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