

The Rianta Solutions RS4100 40/100G Ethernet MAC/PCS/PMA block is fully verified IP suitable for integration into FPGA or ASIC solutions for multiple packet applications. Implemented in Verilog with comprehensive testbench support, the RS4100 includes a complete dual rate MAC and PCS/PMA, complete with RMON/MIB statistics and Ethernet OAM support.

Interfaces

- System Data
 - Flexible Rx and Tx Data Packet FIFOs
- PMD Lanes
 - 4x10.3125 GBd for 40G
 - 10x10.3125 GBd or 4x25.78125 GBd for 100G
- Management
 - Serial or parallel Address/Data
 - Access to EOAM Tx/Rx FIFOs

Applications

- Packet Processing
 - Switching
 - Routing
- Packet Transport
 - Packet Optical Transport Systems (POTS)

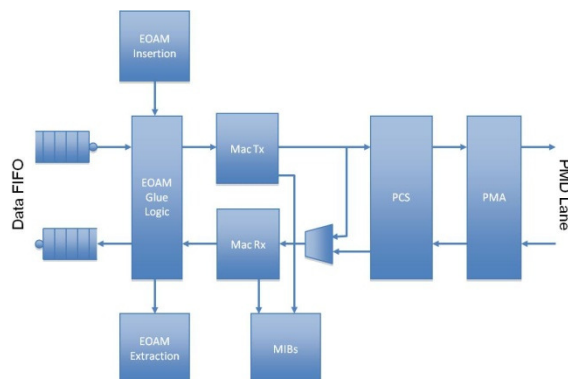
RS4100

40/100G Ethernet MAC/PCS/PMA

Features

- Dual-rate PMA
 - 20 PCS Lanes
 - 4x10G, 10x10G or 4x25G PMD lanes
 - Full bit multiplexing/demultiplexing
 - XLAUI/CAUI support
- Dual-rate PCS
 - 40/100Gbit/s operation
 - 64B/66B encoding/decoding
 - Scramble/descramble
 - Alignment insertion/removal
 - Block distribution/lane reordering
 - Lane block sync and deskew
 - Auto-negotiation
 - Detection and generation of fault and control codes
 - Full duplex
- Dual-rate MAC
 - Wire speed CRC-32 verification in Rx direction
 - Optional frame discard on failure
 - Optional CRC-32 insertion in Tx direction
 - PAUSE Frame based flow control
 - Automatic generation based on configurable Rx FIFO thresholds
 - S/W controlled generation
 - Configurable PAUSE quanta
 - 64-16000 byte frame size
 - Full RMON MIB statistics
 - Ethernet OAM frame insertion and capture
 - Flexible capture match field with bit mask
 - Covers DA, Type/Info, Q tag

Block Diagram



Description

The Rianta Solutions RS4100 40/100G Ethernet MAC/PCS/PMA is a flexible IP core which can be integrated into a variety of applications requiring Ethernet connectivity. Providing a combined MAC, PCS and PMA implementation, the RS4100 can interface directly to a PMD or XLAUI/CAUI implementation on the line side, and to any transport or switching function on the system side.

The PMD Lane interface can be configured for 4x10G, 10x10G or 4x25G lanes to simplify multi-rate designs. On the system side, simple transmit and receive FIFOs are provided with configurable thresholds for automatic flow control along with access to absolute pointer locations to manage fill levels. Parallel and serial control interfaces are also provided for access to all control and status registers as well as EOAM insertion/extraction buffers.

Implemented in Verilog RTL, the RS4100 is fully verified with a high level test suite that can also be integrated into system test scenarios.

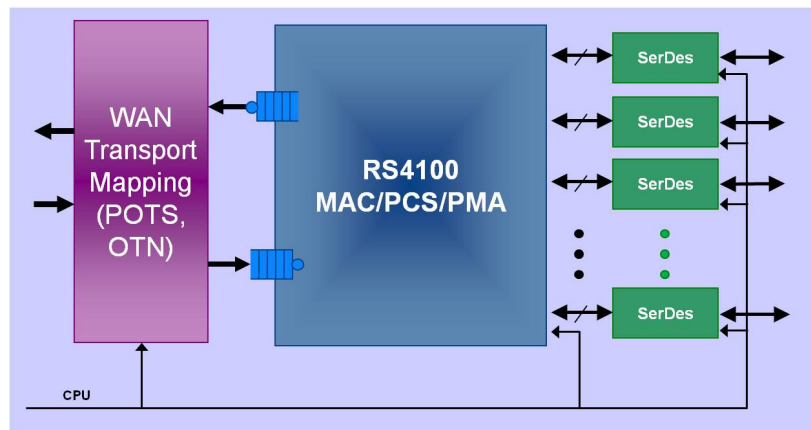


Figure 1: 40/100G Ethernet Transport

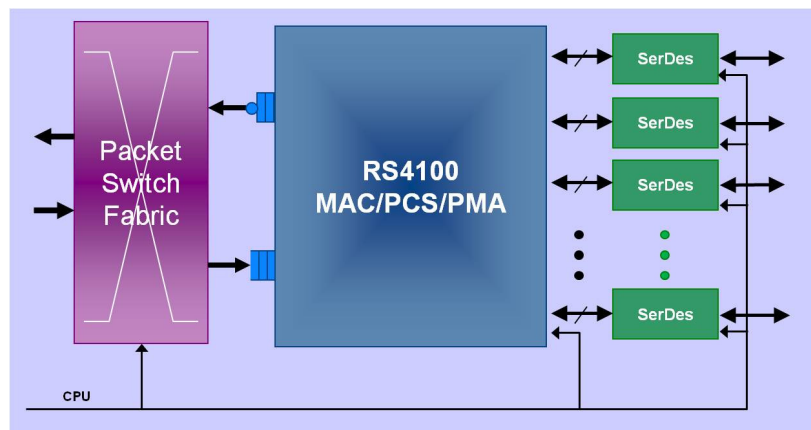


Figure 2: 40/100G Ethernet Switching

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