

The Rianta Solutions RS5100 100G OTU4 Framer block is fully verified IP suitable for integration into FPGA or ASIC solutions for multiple transport applications. Implemented in Verilog with comprehensive testbench support, the RS5100 includes a flexible OTL Multi-Lane interface, complete OTU4/ODU4 framing and overhead processing, and 100G client to OPU4 mapping support.

Interfaces

- System Data
 - Flexible Rx and Tx Data FIFOs
- Optical Transport Lanes
 - OTL4.4: 4 x 21.883 Gb/s
 - OTL4.10: 10 x 11.181 Gb/s
- Management
 - Serial or parallel Address/Data

Applications

- OTN Multiplexing
 - OTU4 Network Line Interface
- OTN Switching
 - OTU4 Line interfaces
 - OTU4 Tributary interfaces
- Packet Optical Transport
 - 100GBASE-R OTN mapping

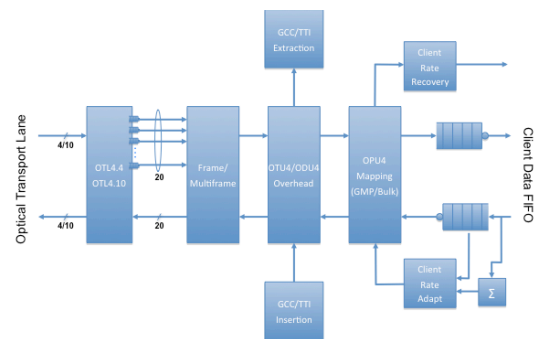
RS5100

100G OTU4 Framer

Features

- Flexible Optical Transport Lane (OTL) interface
 - 4x10G Physical Lanes (OTL4.4)
 - 10x10G Physical Lanes (OTL4.10)
 - Multiplex/Demultiplex from/to 20 Logical Lanes
 - Full Logical Lane framing, deskew and reordering on receive
- OTU4/ODU4 Framing
 - Frame/Multiframe Alignment
- OTU4 Overhead processing
 - Section Overhead generation and monitoring
 - TTI, BIP, BEI/BIAE, BDI, IAE
 - GCC interface to MPU
- ODU4 Overhead Processing
 - ODU4 Path and full ODU4 Tandem Connection (x6) monitoring and generation
 - TTI, BIP, BEI/BIAE*, BDI, STAT, DM (*BIAE for TCM only)
 - GCC1, GCC2 interface to MPU
 - APS/PCC
- OPU4 Mapping
 - Generic Mapping Procedure (GMP) mapping
 - Based on received client word count per frame or FIFO fill level monitoring
 - Cm and Σ Cnd processing (m=640, n=8)
 - Client rate recovery
 - Bulk mapping without rate adaption
 - e.g. GFP-F frames

Block Diagram



Description

The Rianta Solutions RS5100 100G OTU4 Framer is a flexible IP core that can be integrated into a variety of applications requiring 100G OTU4 interfaces. Providing a combined Optical Transport Lane and OTU4/ODU4 implementation, the RS5100 can interface directly to multiple SerDes on the line side, and to any client signal interface on the system side.

The Optical Transport Lane interface can be configured for OTL4.4 (4 x 25G) or OTL4.10 (10x10G) for flexibility in interfacing to a variety of external optics modules. On the system side, simple transmit and receive FIFOs are provided that support both bulk (full rate of OPU4 payload) and GMP based rate adapted (client rate less than OPU4 payload) mapping. For GMP, rate adaptation can be controlled with configurable thresholds or direct client word count information. Parallel and serial control interfaces are also provided for access to all control and status registers as well as TTI and GCC insertion/extraction buffers.

Implemented in Verilog RTL, the RS5100 is fully verified with a high-level test suite that can also be integrated into system test scenarios.

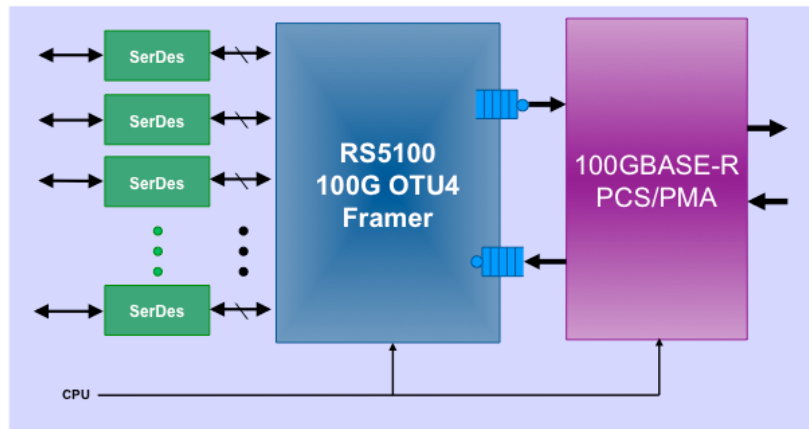


Figure 1: 100G Ethernet Transport

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